WAFER SCALE STRUCTURE FOR PROGRAMMABLE LOGIC

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Abstract of **JP7066718**
PURPOSE: To provide an FPLA improving adaptivity to the integration of wafer scale. CONSTITUTION: Concerning logic and routing cells for constructing a programmable gate array, this gate array is constituted by arranged logic and routing cell units on the surface of wafer in the form of tile. This logic and routing cell is provided with both logic cells 12-19 and routing circuits 20-27 and by connecting the logic cells to all the levels of hierarchical routing system, the connection among various logic cells is achieved.